**Unit I**

**Short Answers:**

1. Define Threshold Voltage and write its equation
2. Prove that if thickness of oxide increases then threshold voltage increases.
3. Write short notes on velocity saturation
4. What is the difference between thin oxide and thick oxide?
5. Write short notes on photolithography with neat sketch
6. Define Channel Length modulation and sub-threshold conduction
7. Derive the trans conductance, gm of the MOSFET
8. Discuss the Body effect in MOSFETs
9. What is Latch-up in CMOS circuits how to avoid it.
10. Write about simple MOS Capacitance model.

**Long Answers**

1. Explain the construction, operation and characteristics of Enhancement n-channel

MOSFET using neat sketches.

1. Explain the CMOS fabrication process using P-Well & N-Well with neat diagrams.
2. Derive Ids equation for n-channel MOSFET operating in linear and saturation regions
3. Explain NMOS fabrication process in detail with neat sketches.
4. Explain the Operation of BiCMOS Inverter and its Fabrication Process.
5. Problems on Ids n Threshold voltage

**Unit II**

2. **Short Answers**
3. Write about the Pseudo NMOS inverter using circuit diagram
4. Discuss power dissipation in CMOS circuits.
5. Draw the 3 input NAND gate using dynamic CMOS logic.
6. Derive the rise time for CMOS inverter
7. What is meant by Ratioed Logic? Give example.
8. Implement 4X1MUX using PTL & Transmission Gate Logic.
9. Why NMOS Depletion Load Inverter is advantage over Enhancement load
10. Write Disadvantages of NMOS Inverter with Resistive load.
11. Write advantages of Dynamic CMOS over Static CMOS.
12. What is the disadvantage of Dynamic CMOS and how to overcome it?

**Long Answers:**

1. Explain the operation of CMOS inverter in detail.
2. Determine the ratio of pull-up to pull-down (Zpu/Zpd) for a NMOS inverter driven by another NMOS inverter.
3. Determine the pull-up to pull-down ratio for a NMOS inverter driven by another NMOS inverter through one or more pass transistors
   1. 4 a) Explain the operation NMOS inverter and its characteristics.

b) Discuss alternative forms of pull-up.

**Unit III**

1. What are the four basic layers of layout/stick diagram.
2. Define Stick Diagram.
3. Stick Diagram of 2-input OR Gate.
4. Draw the stick diagram of 2- input NAND using NMOS design style
5. Draw the schematic, stick diagram and layout for a 2-input CMOS OR gate.
6. Draw the schematic and Stick diagram and Layout for EX-NOR gate using NMOS design style. Draw the schematic, stick diagram and layout for 2 input CMOS AND gate.
7. Draw the schematic and Stick diagram and Layout for EX-OR gate using CMOS design style.

Draw the schematic, stick diagram and layout for y=(AB+CD)’

Draw the schematic, stick diagram and layout forY=(AB+C(D+E)) ‘